What Is Claimed Is:

1. An apparatus for generating quadrature phase signals, comprising:

a base selector having a control input terminal for receiving a region control signal, a plurality of reference clock input terminals respectively for receiving a plurality of reference clock signals of the same frequency and different phases, and four base clock output terminals for outputting a first, a second, a third and a fourth base clock signals, said first, said second, said third and said fourth base clock signals being generated in accordance with said region control signal by using said plurality of reference clock signals, a phase difference between said first and said second base clock signals being substantially equal to a phase difference between said third and said fourth base clock signals, a phase difference between said first and said third base clock signals being substantially 90 degrees, a phase difference between said second and said fourth base clock signals being substantially 90 degrees;

a first phase interpolator having a control input terminal, two phase input terminals for respectively receiving said first and said second base clock signals, and a first output terminal, said first phase interpolator generating a first clock signal at said first output terminal in accordance with a position control signal at said control input terminal, said first clock signal having a frequency equal to the frequency of said first and said second base clock signals and having a phase being a weighted average of the phases of said first and said second base clock signals; and

a second phase interpolator having a control input

terminal, two phase input terminals for respectively receiving said third and said fourth base clock signals, and a second output terminal, said second phase interpolator generating a second clock signal at said second output terminal in accordance with a position control signal at said control input terminal, said second clock signal having a frequency equal to the frequency of said third and said fourth base clock signals and having a phase being a weighted average of the phases of said third and said fourth base clock signals, said first and said second clock signals being substantially 90 degrees out of phase with each other.

2. The apparatus for generating quadrature phase signals of claim 1, wherein said first, said second, said third and said fourth base clock signals are generated by selecting four signals from said plurality of reference clock signals and their inverted signals.

3. The apparatus for generating quadrature phase signals of claim 1, wherein said base selector has four reference clock input terminals for receiving four reference clock signals, the phases of said four reference clock signals and their inverted signals are offset from one another by 45 degrees, and said first, said second, said third and said fourth base clock signals are generated by selecting four signals from said four reference clock signals and their inverted signals.

4. The apparatus for generating quadrature phase signals of claim 3, wherein the phase difference between said first and said second base clock signals is substantially 45 degrees and the phase difference between

said third and said fourth base clock signals is substantially 45 degrees.

5. An apparatus for generating quadrature phase signals, comprising:

a base selector, comprising:

a buffer/inverter unit having four input terminals, four corresponding control terminals and four corresponding output terminals, said buffer/inverter unit receiving a first, a second, a third and a fourth reference clock signals of the same frequency and different phases respectively at said four input terminals and outputting four signals selected from said first, said second, said third and said fourth reference clock signals and their inverted signals respectively at said four corresponding output terminals based on control signals at said four corresponding control terminals; and

a bypass/cross unit including a first and a second bypass/cross multiplexers, each of said multiplexers having two input terminals, two output terminals and a control terminal, said first bypass/cross multiplexer having its two input terminals connected to two of said four output terminals of said buffer/inverter unit and outputting a first and a third base clock signals by either direct-connecting or cross-connecting signals at its two input terminals to its two output terminals in accordance with a control signal at its control terminal, said second bypass/cross multiplexer having its two input terminals connected to the other two of said four output terminals of said buffer/inverter unit and outputting a second and a fourth base clock signals

by either direct-connecting or cross-connecting signals at its two input terminals to its two output terminals in accordance with a control signal at its control terminal, a phase difference between said first and said second base clock signals being substantially equal to a phase difference between said third and said fourth base clock signals, a phase difference between said first and said third base clock signals being substantially 90 degrees, a phase difference between said second and said fourth base clock signals being substantially 90 degrees;

a first phase interpolator having a control input terminal, two phase input terminals for respectively receiving said first and said second base clock signals, and a first output terminal, said first phase interpolator generating a first clock signal at said first output terminal in accordance with a position control signal at said control input terminal, said first clock signal having a frequency equal to the frequency of said first and said second base clock signals and having a phase being a weighted average of the phases of said first and said second base clock signals; and

a second phase interpolator having a control input terminal, two phase input terminals for respectively receiving said third and said fourth base clock signals, and a second output terminal, said second phase interpolator generating a second clock signal at said second output terminal in accordance with a position control signal at said control input terminal, said second clock signal having a frequency equal to the frequency of said third and said fourth base clock signals and having a phase being a weighted average of the phases of said third

and said fourth base clock signals, said first and said second clock signals being substantially 90 degrees out of phase with each other.

6. The apparatus for generating quadrature phase signals of claim 5, wherein said buffer/inverter unit of said base selector comprises a plurality of XOR (Exclusive-Or) gates.

7. The apparatus for generating quadrature phase signals of claim 6, wherein said buffer/inverter unit of said base selector comprises four XOR (Exclusive-Or) gates, each having two input terminals, respectively used as one of said four input terminals of said buffer/inverter unit for receiving one of said reference clock signals and as one of said four corresponding control terminals of said buffer/inverter unit for receiving one of said corresponding control signals.

8. The apparatus for generating quadrature phase signals of claim 5, wherein the phases of said first, said second, said third and said fourth reference clock signals and their inverted signals are offset from one another by 45 degrees.

9. The apparatus for generating quadrature phase signals of claim 8, wherein the phase difference between said first and said second base clock signals is 45 degrees and the phase difference between said third and said fourth base clock signals is 45 degrees.

10. A data recovery circuit, comprising:

a phase detector receiving an incoming data signal and a first and a second clock signals, said first and said second

clock signals having a frequency equal to half the frequency of said incoming data signal and being substantially 90 degrees out of phase with each other, said phase detector comparing the phase of said incoming data signal with the phase of said second clock signal and accordingly generating a phase error signal if a phase difference exists between said incoming data signal and said second clock signal while generating an output data signal recovered from said incoming data signal with said first clock signal if no phase difference exists between said incoming data signal and said second clock signal;

a loop filter receiving said phase error signal from said phase detector and accordingly generating a region control signal and a position control signal for adjusting the phases of said first and said second clock signals;

a multiphase clock source for generating a plurality of reference clock signals of the same frequency and different phases from an external clock signal; and

a quadrature phase generator receiving said region control signal and said position control signal from said loop filter and said plurality of reference clock signals from said multiphase source and generating said first and said second clock signals for outputting to said phase detector, said quadrature phase generator comprising:

a base selector for generating a first, a second, a third and a fourth base clock signals in accordance with said region control signal by using said plurality of reference clock signals, a phase difference between said first and said second base clock signals being substantially equal to a phase difference between said third and said fourth base clock signals, a phase difference between said first and said third base clock

signals being substantially 90 degrees, a phase difference between said second and said fourth base clock signals being substantially 90 degrees;

a first phase interpolator receiving said first and said second base clock signals and generating a first clock signal in accordance with said position control signal, said first clock signal having a phase being a weighted average of the phases of said first and said second base signals; and

a second phase interpolator receiving said third and said fourth base clock signals and generating a second clock signal in accordance with said position control signal, said second clock signal having a phase being a weighted average of the phases of said third and said fourth base signals.

11. A data recovery circuit, comprising:

a phase detector receiving an incoming data signal and a first and a second clock signals, said first and said second clock signals having a frequency equal to half the frequency of said incoming data signal and being substantially 90 degrees out of phase with each other, said phase detector comparing the phase of said incoming data signal with the phase of said second clock signal and accordingly generating a phase error signal if a phase difference exists between said incoming data signal and said second clock signal while generating an output data signal recovered from said incoming data signal with said first clock signal if no phase difference exists between said incoming data signal and said second clock signal;

a loop filter receiving said phase error signal from said phase detector and accordingly generating a region control

signal and a position control signal for adjusting the phases of said first and said second clock signals;

a multiphase clock source for generating a first, a second, a third and a fourth reference clock signals of the same frequency and different phases from an external clock signal; and

a quadrature phase generator receiving said region control signal and said position control signal from said loop filter and said four reference clock signals from said multiphase source and generating said first and said second clock signals for outputting to said phase detector, said quadrature phase generator comprising:

a base selector, comprising:

a buffer/inverter unit receiving said four reference clock signals and selectively outputting four signals selected from said first, said second, said third and said fourth reference clock signals and their inverted signals respectively at its four output terminals in accordance with said region control signal; and

a first and a second bypass/cross multiplexers, said first bypass/cross multiplexer generating a first and a third base clock signals by either direct-outputting or cross-outputting signals at two of the four output terminals of said buffer/inverter unit in accordance with said region control signal, said second bypass/cross multiplexer generating a second and a fourth base clock signals by either direct-outputting or cross-outputting signals at the other two of the four output terminals of said buffer/inverter unit in accordance with said region control signal, a phase

difference between said first and said second base clock signals being substantially equal to a phase difference between said third and said fourth base clock signals, a phase difference between said first and said third base clock signals being substantially 90 degrees, a phase difference between said second and said fourth base clock signals being substantially 90 degrees;

a first phase interpolator receiving said first and said second base clock signals and generating a first clock signal in accordance with said position control signal, said first clock signal having a phase being a weighted average of the phases of said first and said second base signals; and

a second phase interpolator receiving said third and said fourth base clock signals and generating a second clock signal in accordance with said position control signal, said second clock signal having a phase being a weighted average of the phases of said third and said fourth base signals.

12. The data recovery circuit of claim 11, wherein said buffer/inverter unit of said base selector comprises four XOR (Exclusive-Or) gates, each having two input terminals respectively for receiving one of said reference clock signals and for receiving one bit of said region control signal.

13. The data recovery circuit of claim 11, wherein the phases of said first, said second, said third and said fourth reference clock signals and their inverted signals are offset from one another by 45 degrees.

14. The data recovery circuit of claim 13, wherein the phase difference between said first and said second base clock signals is substantially 45 degrees and the phase difference between said third and said fourth base clock signals is substantially 45 degrees.